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IMPLEMENTATION OF HIGH STEP-UPDC-DC CONVERTER FOR LOWVOLTAGEPHOTO VOLTAIC SYSTEM

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ABSTRACT

This paper proposes a high Step-up DC-DC converter with dual active clamping circuit. The proposed converter has the dual active clamping circuit which is developed based on the conventional active clamp circuit. The proposed converter consists of two parallel-connected transformers for dual active clamping to reduce the voltage stresses of the semiconductor devices. Conventional converter has the active clamping circuit due to that voltage stresses of the semiconductor devices are considerably high. The proposed converter has low switching power losses and high power efficiency. The use of parallel-connected two transformers gives a low-profile design for the step-up DC-DC converter. The proposed converter is an attractive design for alternative low dc voltage energy sources, such as solar photovoltaic modules. The proposed system will be simulated in MATLAB/SIMULINK environment to determine the effectiveness of the proposed system.

1.INTRODUCTION

The power generation systems using low-DC renewable energy sources such as photovoltaic module and fuel cell need a high step-up DC-DC converter to interface the low-DC voltage to the high DC voltage distribution network . Lots of efforts have been made to develop high step-up DC-DC converters with a high efficiency. Among the investigated topologies, the active-clamped step-up DC-DC converters are gaining its popularity, thanks to its high step-up ratio and soft-switching operation. The active clamped step-up DC-DC converter has a high step-up gain by using the active-clamp circuit at the primary side and the voltage doublers rectifier at the secondary side. Moreover, the series-resonance between the transformer leakage inductor and the capacitor in the voltage doublers rectifier makes the output diodes to be turned off at zero current condition. However, the power switches at the primary side operate under hard-switching condition, which still causes high switching power losses and high heat dissipation problems. To address these drawbacks, this paper proposes the dual active-clamped step-up DC-DC converter where the voltage stresses of the semiconductor devices can be reduced. The proposed converter in Fig. 1 has the dual active-clamping circuit with parallel-connected two transformers. Compared to the previous active-clamped step up DC-DC converters, the voltage stresses of the power switches at the primary side are reduced by the dual active clamping circuit. Moreover, by using parallel-connected two transformers, two voltage doublers rectifier circuits are equipped, which reduces the voltage stress of each output diode by half. The proposed converter reduces the switching power losses by reducing the voltage stresses of the semiconductor devices. The performance of the proposed converter is verified from 350 W (350 V / 1 A) experimental prototype circuit for 50 V photovoltaic module voltage.

1.1. SOLAR CELL SYSTEM

A solar cell (also called photovoltaic cell or photoelectric cell) is a solid state electrical device that converts the energy of light directly into electricity by the photovoltaic effect Which Is Shown In Fig 1.3.Assemblies of solar cells are used to make solar modules which are used to capture energy from sunlight. When multiple modules are assembled together (such as prior to installation on a pole-mounted tracker system), the resulting integrated group of modules all oriented in one plane is referred to in the solar industry as a solar panel. The electrical energy generated from solar modules, referred to as solar power, is an example of energy. Photo is the field of technology and research related to the practical application of photovoltaic cells in producing electricity from light, though it is often used specifically to refer to the generation of electricity from sunlight. Cells are described as photovoltaic cells when the light source is not necessarily sunlight (lamplight, artificial light, etc.). These are used for detecting light or other electromagnetic radiation near the visible range, for example infrared detectors, or measurement of light intensity.

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Fig 1.1 Diagram of Solar Panel.

1.2. MPPT METHODS

1.2.1 Characteristics of the PV module

As previously mentioned, the characteristics of the PV module vary with different irradiation levels and ambient temperatures. A simplified equivalent circuit in Fig. 2 can facilitate the investigation of the nonlinear behaviors of the PV module. The equivalent circuit consists of a current source I_L, which suggests the light-generated current; a diode D_1, which emulates the PN junction of a real PV cell; a series resistor R_S and a parallel resistor R_P which symbolize the parasitic series resistance and parasitic parallel resistance on the PV module. The voltage generated at terminals P_{PV} is the voltage of the PV module, which can be multiplied through series-connected PV modules. Moreover, the current outflow from terminals I_{PV} is the current of the PV module.

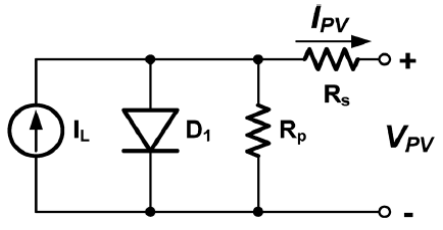

Fig. 1.2. Equivalent circuit of the PV module.

The relationship between V_{PV} and I_{PV} can be shown in the following equations,

$$I_{PV} = I_L - I_{os}\left\{\exp\left[\frac{q}{AkT}(V_{PV} + I_{PV}R_s)\right] - 1\right\} - \frac{V_{PV} + I_{PV}R_s}{R_P}$$

$$I_{os} = I_{or}\exp\left[\frac{qE_{GO}}{Bk}\left(\frac{1}{T_r} - \frac{1}{T}\right)\right]\left[\frac{T}{T_r}\right]^3$$

$$I_L = \frac{S\left[I_{SC} + K_I(T - 25)\right]}{100}$$

I_{PV}	PV module output current;
V_{PV}	PV module output voltage;
R_p	parallel resistor;
R_s	series resistor;
I_{os}	PV module reversal saturation current;
A, B	ideality factors;
T	temperature (°C);
k	Boltzmann's constant;
I_L	light-generated current;
q	electronic charge;
K_I	short-circuit current temperature coefficient at I_{SC};
S	solar irradiation (W/m^2);
I_{SC}	short-circuit current at 25°C and 1000 W/m^2;
E_{GO}	bandgap energy for silicon;
T_r	reference temperature;
I_{or}	saturation current at temperature T_r.

The equations verify that the characteristics of the PV module depend on temperature and solar irradiation level. Fig. 3 shows the IV curves plotted under different irradiation levels and ambient temperatures. Under different irradiation levels [Fig. 3(a)], maximum power point P_{MPP} increases nonlinearly as solar irradiation increases. On the other hand, under different ambient temperatures, the characteristics of the IV curves of the solar array behave in the manner depicted in Fig. 3(b). A nonlinear decrease in P_{MPP} is observed when ambient temperature increases. These nonlinear characteristics of the PV module are crucial for analyzing and designing the PV system, especially for the MPP tracker.

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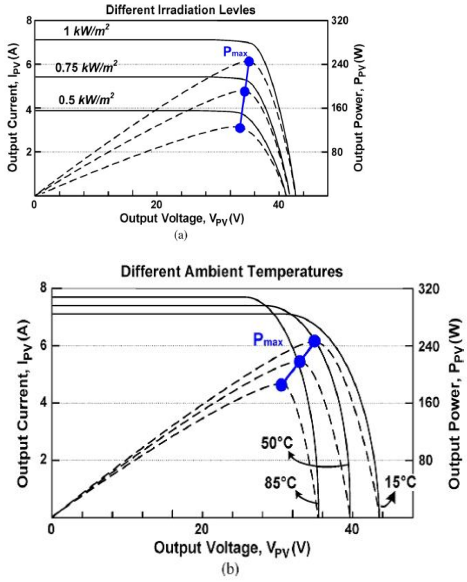

Fig.1.3. Characteristic curves under (a) different irradiation levels and (b) ambient Temperatures.

1.1 MPPT ALGORITHM

Fig. 4 demonstrates the concept of the proposed MPPT algorithm. Before the solar power system is activated, the operating point of the system is located on open-circuit voltage point V_{OC}. Conventional MPPT algorithms, such as slope detection algorithm [e.g., perturbation and observation (P&O) algorithm or hill-climbing (HC) algorithm], calculate the slope of the characteristic curves to determine slope conditions and track the MPP. Nevertheless, a PV system adopting this algorithm requires a lengthy amount of time to track the operating point from V_{OC} to MPP during the system power-on period, as depicted in Fig. 4.

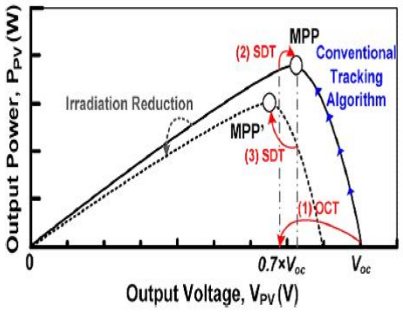

Fig. 1.4. Illustration of the proposed MPP tracking algorithm.

Other tracking algorithms such as the constant voltage algorithm use a fixed ratio of maximum power voltage to open-circuit voltage V_{OC} to approximate the MPP. Theoretically, 0.7 fractions of open-circuit voltage V_{OC} is close to the MPP [32]. Therefore, periodically disconnecting the solar array and power stage to measure V_{OC} and multiplying it to 0.7 can rapidly detect the current MPP. The fraction factor (0.7) varies when different. Solar cell materials are used. In this sense, the MPP cannot be guaranteed when varying environmental conditions are taken into consideration. Moreover, consistent disconnection between the solar array and power stage causes power delivery interruption during the sampling period, thereby resulting in the low power efficiency of the PV system.

To increase tracking speed and accuracy while maintaining high power efficiency, the open-circuit tracking (OCT) and slope detection tracking (SDT) algorithms are adopted to track the MPP in this study. Disconnection between the solar array and power stage occurs only once; that is, at the beginning of the system power-on period. This way, unnecessary power loss is avoided and the power efficiency is maintained. Fig. 6 illustrates the timing diagram of the proposed tracking algorithm.

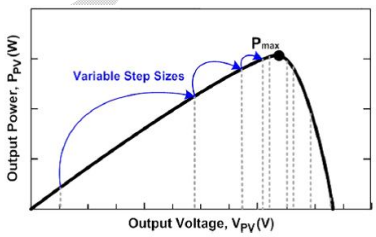

Fig. 1.5. Illustration of the variable step perturbation (VSP) technique.

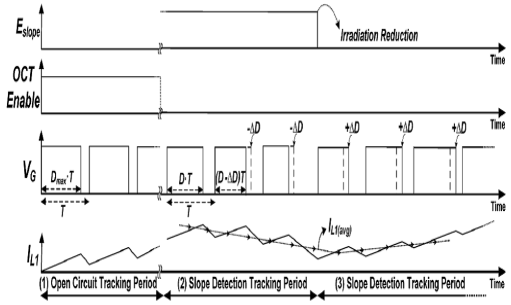

Fig.1.6. Timing diagram of the proposed MPP tracking algorithm.

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E_{slope} is a digital signal meant to indicate the slope condition Logic-high E_{slope} means that the slope condition of the solar array is positive. By contrast, logic-low E_{slope} means dP_{PV}/dV_{PV} is negative. OCT Enable indicates whether the OCT algorithm is enabled. V_G is the gate signal of the power NMOS in the boost converter. Signal I_{L1}shows the inductor current of the boost converter, which can also indicate the current of the solar array. The tracking procedure can be divided into the following is a digital signal meant to indicate the slope condition.

Logic-high means that the slope condition of the solar array is positive. By contrast, logic-low means is negative. OCT Enable indicates whether the OCT algorithm is enabled. is the gate signal of the power NMOS in the boost converter. Signal shows the inductor current of the boost converter, which can also indicate the current of the solar array. The tracking procedure can be divided into the following sequences.

First, before the solar power system is activated, V_{OC} is detected by the controller to set the solar array voltage V_{PV} close to $0.7*V_{OC}$. This approach improves tracking speed unlike the slow tracking speeds in conventional P&O and HC algorithms. The switching duty cycle of the boost converter is set to its maximum value to accelerate the tracking speed during the open-circuit voltage detection period. Second, after the OCT period, the SDT technique takes over the tracking procedure to continually and accurately track the MPP, ensuring that the power stage receives the most energy from the solar array. Third, when environmental conditions change (e.g., reduction in irradiation level), the slope condition changes from positive to negative, as indicated by the solar cell characteristics shown in Fig. 3.

PV voltage tends to decrease as PV Subsequently; the SDT technique consistently monitors the slope condition and guarantees that the system operates at the MPP regardless of any environmental change. Besides, the SDT algorithm includes the variable step perturbation (VSP) technique [Fig.] to accelerate the tracking speed and to minimize the oscillation problem around the MPP. The system chooses larger perturbation step sizes when the operating point is far away from the MPP, which can increase the tracking speed. In contrast, when the operating point is working around the MPP, the step sizes are set to be smaller in order to minimize the oscillation problem around the **MPPT.**

The AMPPT technique includes the advantages of both the OCT and SDT techniques. The OCT technique can roughly locate the MPP at rapid tracking speeds, while the SDT technique can improve tracking accuracy, which cannot be guaranteed solely by the OCT technique. For a large-scale PV system, unavoidable shadows caused by nearby trees, clouds, and buildings frequently degrade the energy of the solar array. The so-called "partial shading effect" current increases, and vice versa. Thus, the SDT technique increases the switching duty cycle. The current of the solar array increases to reduce the operating voltage and ensure the movement of the system operating point to a new maximum power point, as illustrated in Fig. The flowchart in Fig. summarizes the overall tracking topology of the MPP tracking algorithm. After the solar power system is switched on, the OCT technique is enabled until the operating voltage is set to $0.7*V_{OC}$. Poses a considerable threat to highly efficient energy utilization.

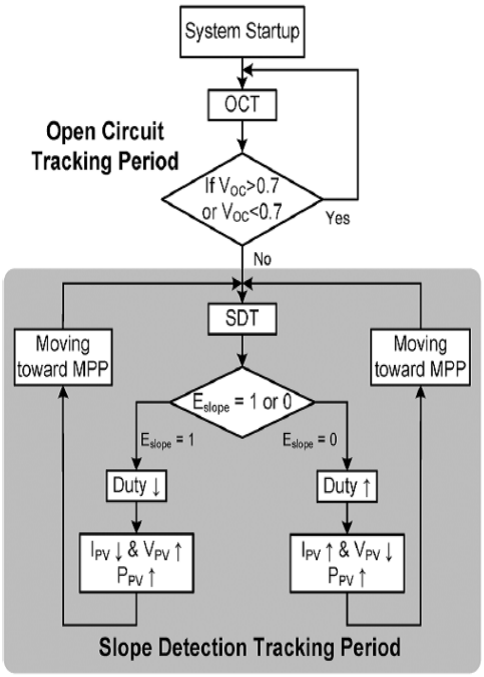

Fig 1.7.flow chart of slope detection method

Perturbation and Observation Algorithm

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Perturbation and Observation (P&O) method has a simple feedback structure and fewer measured parameters. It operates by periodically perturbing (i.e. incrementing or decreasing) the array terminal voltage and comparing the PV output power with that of the previous perturbation cycle. If the perturbation leads to an increase (decrease) in array power, the subsequent perturbation is made in the same (opposite) direction. In this manner, the peak power tracker continuously seeks the peak power condition. MPP is tracked by using DC-DC converters. Much attention has been given to the High boost ratio hybrid transformer topology recently because output voltage must be higher than input voltage .The output is also not inverted as is the case in a fly back or Cuk topology. The input and output voltages are DC isolated by a coupling capacitor and the converter works with constant frequency PWM.Fig shows the proposed MPPT algorithm.

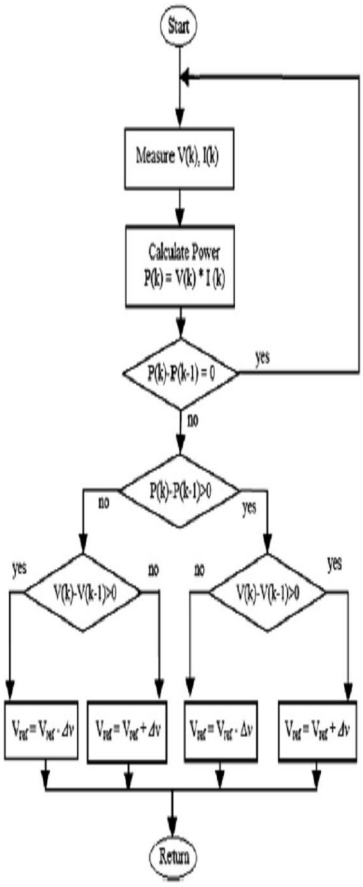

Fig 1.8 Flow chart of P&O MPPT algorithm.

1.5 CONTROLLER DESIGN

1.5.1. DESIGN OF PI REGULATOR

In the design of single-phase rectifier control system, the general use is dual-loop control, namely, voltage and current loops. The outer voltage loop controls the voltage in DC side, while the current loop as the inner loop, it forces the input current tracking current instruction (gained from the output of the outer voltage loop), in order to achieve sinusoidal current control unity power factor. The current instruction and grid-side voltage have same frequency and opposite phase. Assuming that the input current in grid side can track current instruction completely, the first case is that the grid outputs energy to the load; the second case is that the load outputs energy back to the grid.

1.5.2. The design of inner current loop

The control performance of input current is the key of rectifier control, because the essence of the rectifier is an energy conversion system between the AC and DC power, the grid voltage is essentially certain, so the rapid and effective control of the input current is important. The block diagram of PI regulator in current loop is shown in Figure

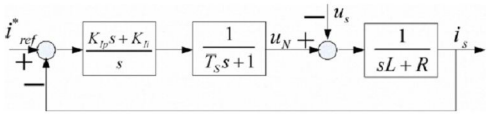

Fig.1.9 The block diagram of transfer function in current loop

The open loop transfer function is shown as follow

$$G_{op}(s)=\frac{(K_{Ip}s+K_{Ii})}{s(T_S s+1)(sL+R)}$$

When the switching frequency is high (e.g., 10k Hz), the first-order inertia loop 1/(TsS +1) is approximately 1 , could be ignored, the type can be simplified to

$$G_{op}(s)=\frac{(K_{Ip}s+K_{Ii})}{s(sL+R)}$$

1.5.3.The design of outer voltage loop

If the filter capacitor of DC side is large enough, the DC voltage ripple can be ignored. The block diagram of PI regulator in voltage loop is shown in Figure.

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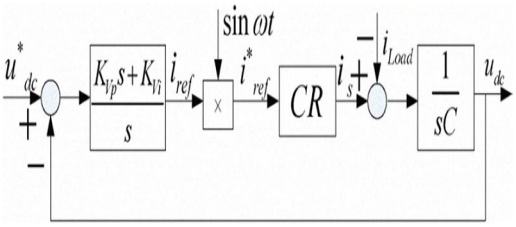

Fig.1.10. The block diagram of transfer function working in voltage loop

The open-loop transfer function is shown as follow

$$G_{opV}(s)=\frac{K_{Vp}s+K_{Vi}}{s}\frac{1}{sC}G_{cl}(s)=\frac{\frac{K_{Vi}}{C}\left(\frac{K_{Vp}}{K_{Vi}}s+1\right)}{s^2}G_{cl}(s)$$

In the above function, Gcl (s) is equivalent to the current closed-loop transfer function

1.5.4. Sinusoidal Pulse width modulation

The switches in the voltage source inverter (Fig.3-3) can be turned on and off as required. In the simplest approach, if the top switch is turned on and off only once in each cycle, a square wave waveform results. However, if turned on several times in a cycle an improved harmonic profile may be achieved.

In the most straightforward implementation, generation of the desired output voltage is achieved by comparing the desired reference waveform (modulating signal) with a high-frequency triangular 'carrier' wave as depicted schematically in Fig.3-4. Depending on whether the signal voltage is larger or smaller than the carrier waveform, either the positive or negative dc bus voltage is applied at the output. Note that over the period of one triangle wave, the average voltage applied to the load is proportional to the amplitude of the signal (assumed constant) during **this period.**

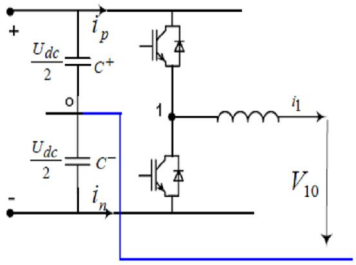

Figure 1.11. Simple Voltage Source Inverter

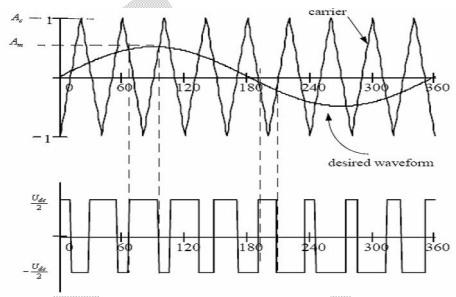

Figure 1.12 Principle of Pulse Width Modulation

2. OPERATION PRINCIPLES

Fig shows the circuit diagram of the proposed dc–dc converter. The converter consists of main switches (S1 , S4), the dual active-clamping circuit (S2 , S3 , Cc), the transformer T, and the resonant voltage doublers rectifier (Llk , Cr , Do 1 , Do 2). The main switches (S1 , S4) and auxiliary switches (S2 , S3) operate complementarily with a short dead time. All switches are the metal–oxide–semiconductor field-effect transistors. They are considered ideal switches except their body diodes DS 1–DS 4 and output capacitors CS 1–CS 4 . Ci is the input capacitor. Cc is the clamping capacitor. Co is the output capacitor. The capacitors Ci , Cc , and Co are large enough so that their voltages Vi , Vc , and Vo are considered constant, respectively. The transformer T has the magnetizing inductor Lm and leakage inductor Llk with the turns ratio of 1:N, where N=Ns /Np . Llk is assumed to be much smaller than Lm. The capacitor Cr is the resonant capacitor. Cr resonates with the leakage inductor Llk . Thus, the resonant capacitor voltage Vr is not considered constant for one switching period.

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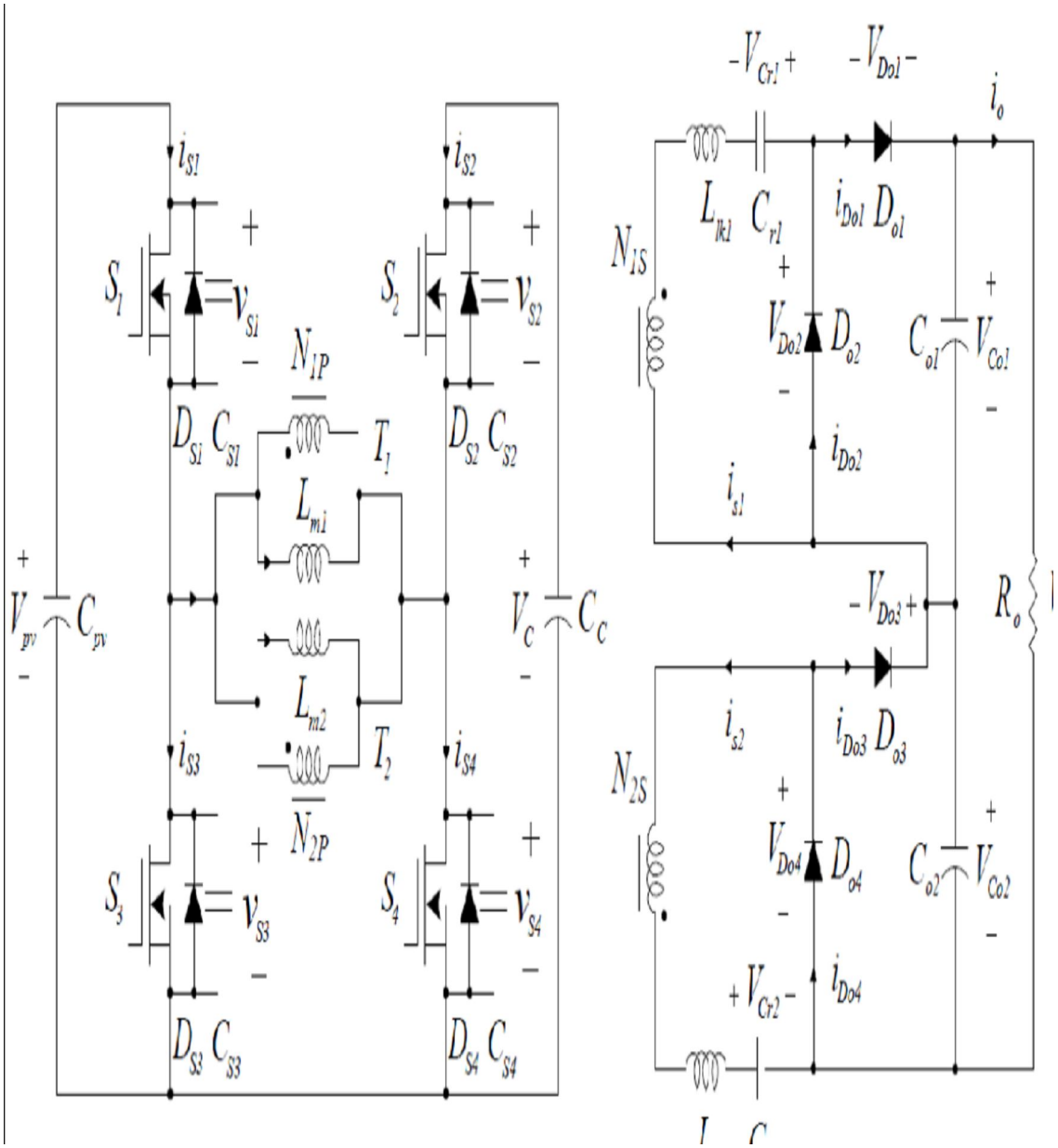

ig 2.1. Circuit diagram of the proposed converter

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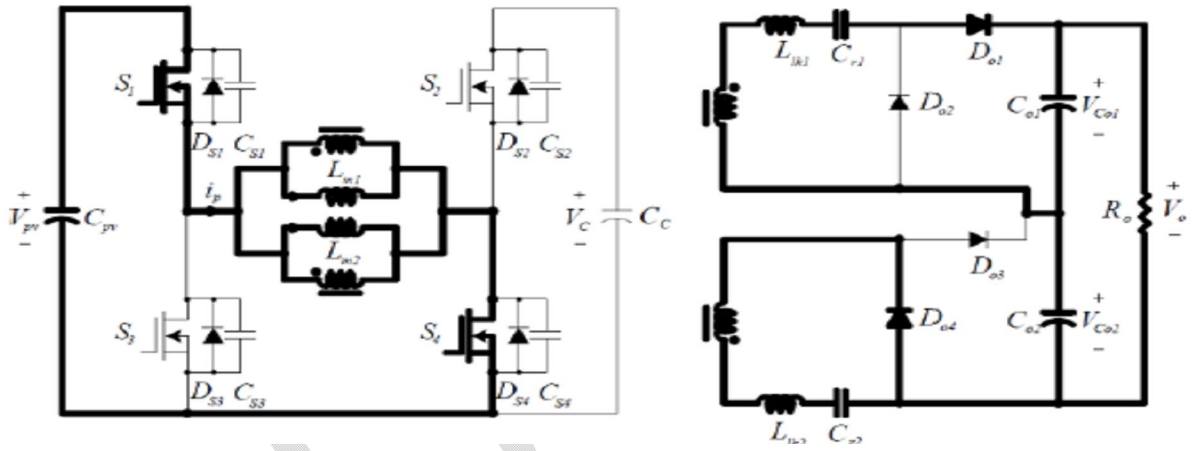
Proposed converter configuration:

Fig. 1 shows the circuit diagram of the proposed converter. The proposed converter has main power switches S1 and S4. The dual active-clamping circuit consists of S2, S3, and Cc. The parallel-connected two transformers T1 and T2 have magnetizing inductor Lm1 and Lm2 and leakage inductors Llk1 and Llk2, respectively. They have the turns ratio as N1P : N1S and N2P : N2S, respectively. The proposed converter has two voltage doubler rectifier circuits Cr1, Do1, Do2, Co1, Cr2, Do3, Do4, and Co2. The leakage inductor Llk1 (Llk2) and the resonant capacitor Cr1 (Cr2) form a series resonance, which makes the output diodes to be turned at zero-current condition. The switches operate at a constant switching period Ts. S1 and S4 are asymmetrically modulated with respect to S2 and S3. Each switch has its own parasitic capacitor and body diode. The switches operate at a constant switching period Ts. Vo is the output voltage as Vo = VCo1 + VCo2. The proposed converter has six distinct operating modes for Ts, as shown in Fig. .

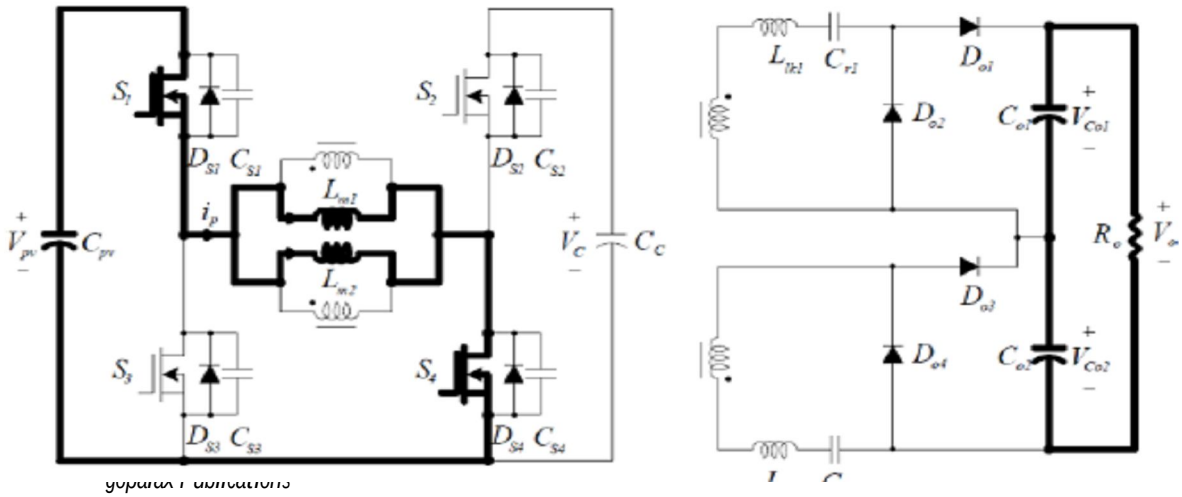
Modes of operation:

Mode 1:

S1 and S4 are turned on at t0. The magnetizing inductors Lm1 and Lm2 store energy from the input power source. The output diodes Do1 and Do4 are turned on at the secondary side. The series resonant circuit consisting of Llk1 (Llk2) and Cr1 (Cr2) is formed, transferring the primary power to the secondary side.



Mode 2:



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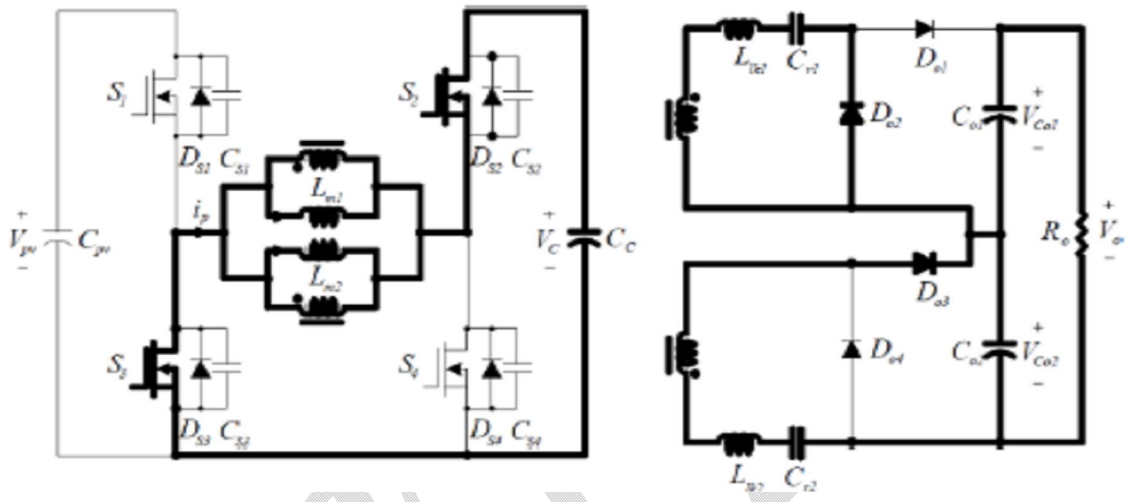
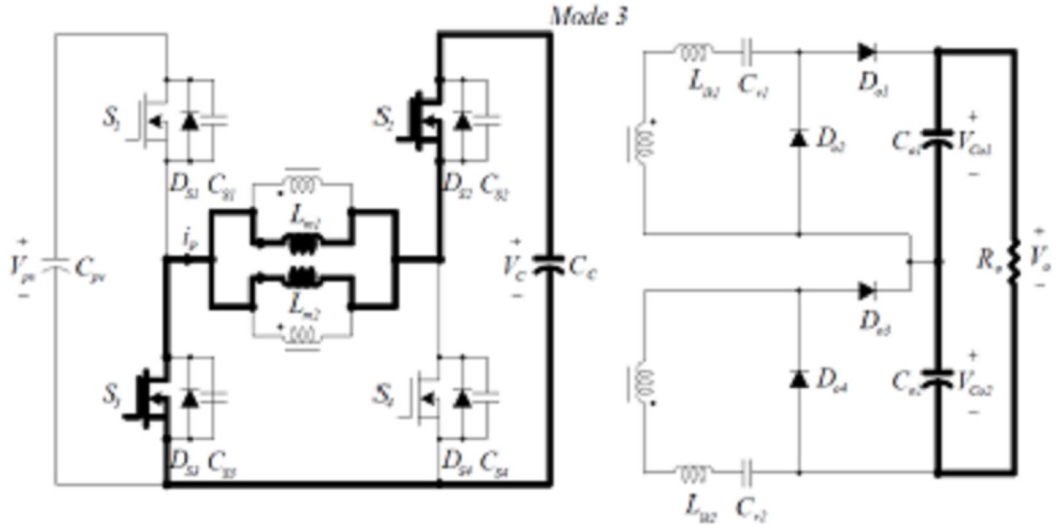
During mode 1 Switch S1, S4 are still ON. The diode currents iDo1 and iDo4 are zero after the half period of the series-resonance. The magnetizing inductors keep storing the energy from the input power source

Mode 3:

S2 and S3 are turned on at t3. The energy stored in the magnetizing inductors is released to the clamping capacitor Cc. The output diodes Do2 and Do3 are turned on at the secondary side. The series resonant circuit consisting of Llk1 (Llk2) and Cr1 (Cr2) is formed, transferring the primary power to the secondary side again.



Mode 4:



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The diode currents iDo2 and iDo3 are zero after the half period of the series-resonance. The magnetizing inductors keep transferring the stored power to the capacitor Cc.

Simulation results:

Fig Simulation circuit of proposed converter

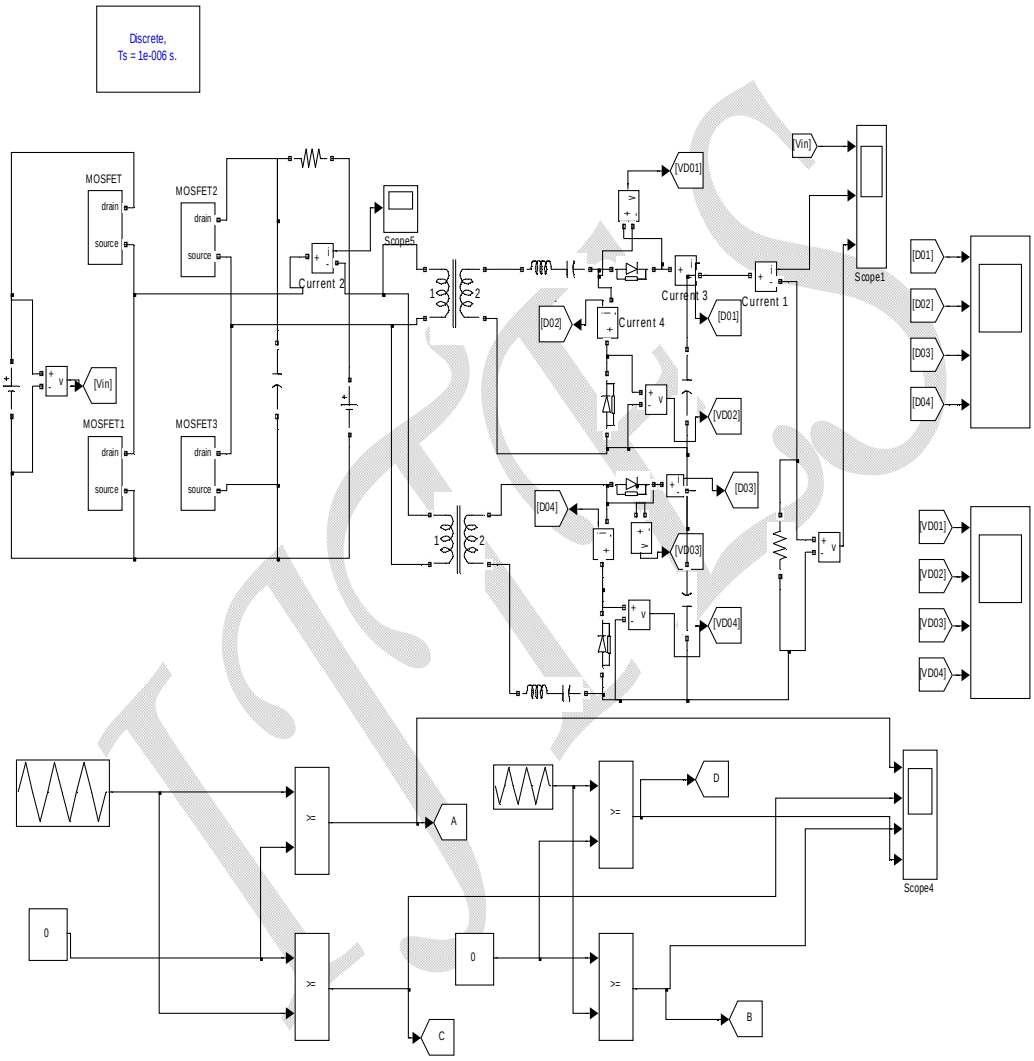

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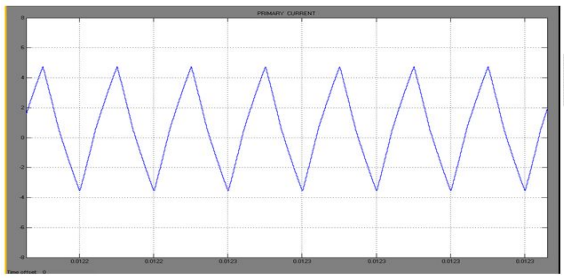
Fig Gate triggering pulse of proposed converter



Transformer primary current waveform

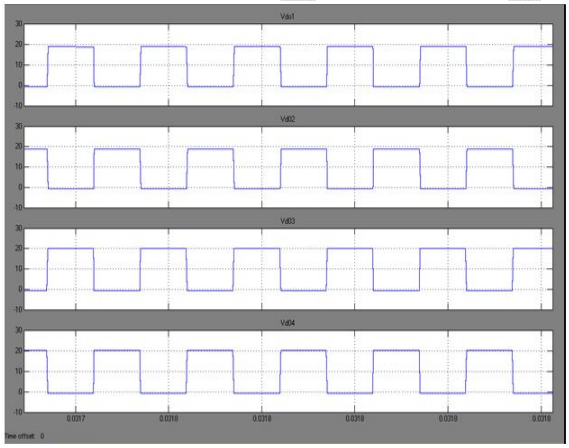


Fig Output diode voltage Do1-Do4

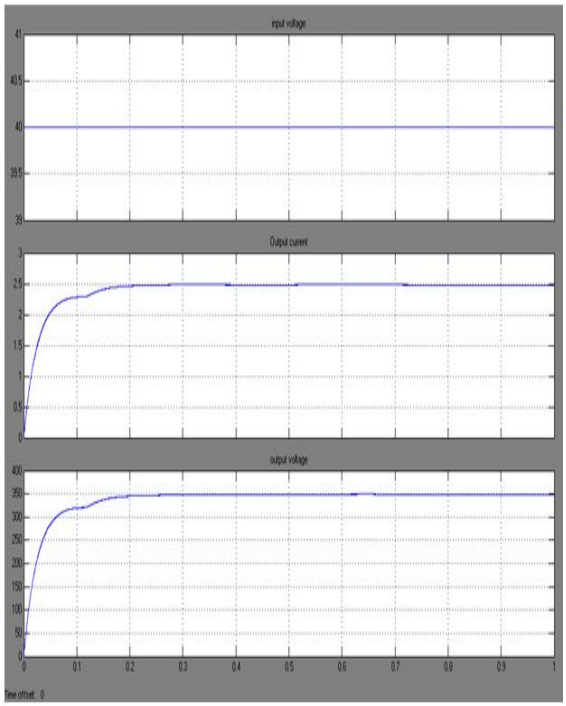


Fig Simulation results of output voltage, current, input voltage waveform of proposed converter

3. CONCLUSION

High Step-up DC-DC converter with Dual active clamping circuit. The proposed converter has the dual active clamping circuit which is developed based on the conventional active clamp circuit. The proposed converter consists of two parallel-connected transformers for dual active clamping to reduce the voltage stresses of the semiconductor devices. Operation principle, analysis, circuit design, Simulation results have been presented in detail. The proposed DC-DC converter achieves low voltage stress of semiconductor switches and attractive design for low voltage photovoltaic energy source.

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